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Design of an 8-bit non-volatile plasmonic memory for synaptic weighting in optical neuromorphic architectures

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ABSTRACT

In this paper, a non-volatile plasmonic memory based on a metal–insulator-metal (MIM) waveguide and phase-change material is proposed to enhance storage density and integration compatibility in photonic integrated circuits (PICs). Silver is utilized as the metal, with its dielectric function characterized by the Drude model, while air and $Ge_2Sb_2Te_5$(GST) serve as the dielectric media. Two-dimensional Finite-Difference Time-Domain (2D-FDTD) simulations demonstrate an operating resonance at λ = 1814 nm, exhibiting an optical contrast of 87 % between phase states, an extinction ratio of ER = 44.04 dB, and an ultra-low insertion loss of 0.60 dB for logic state '1′ (45.60 dB for logic '0′). The cell features all-optical external programmability, non-destructive readout, and ultrafast temporal dynamics in the femtosecond regime (τ_r = 62 fs). By mapping GST phase transitions to quantized optical transmission levels, the proposed architecture functions effectively as a photonic weighting element in optical neural networks to alleviate the von Neumann bottleneck. Generalizing the unit cell yields scalable multi-bit configurations up to 8 bits (256 states), achieving an ultra-high storage density of 4.56 bits/μm^2 within a compact footprint of 0.219 μm^2. Furthermore, a 5-stage CMOS-compatible fabrication workflow (≤200 °C) is presented, and structural sensitivity analysis confirms high fabrication tolerance (ΔER} < 1 dB within a ± 5 nm window).

Introduction

In recent years, with the accelerating growth of global data production, the demand for high-density and low-power-consumption information storage technologies has increased significantly [1]. Classical electronic memory architectures, despite decades of optimization, have reached fundamental physical limits in scalability, speed, and power density [2]. These limitations have highlighted the need for novel memory technologies capable of transcending these boundaries. In this regard, All-Optical Memories, which perform the processes of encoding, storing, and retrieving information entirely within the optical domain, have emerged as a promising solution [3]. Photonics, utilizing light for information processing and transmission, offers high data rates, low latency, and favorable energy efficiency, which has intensified the demand for research into optical and photonic memory technologies [4]. Among the proposed approaches, memories based on Phase Change Materials (PCMs) have secured a unique position due to their reversible structural transitions between crystalline and amorphous phases and their associated optical property changes. Integrating these materials with plasmonic nanostructures has enabled the development of a new generation of high-speed, nanometer-scale, multi-level optical memories [5].

The implementation of all-optical memories is accompanied by several challenges. Silicon-on-Insulator (SOI) platforms are CMOS-compatible but suffer from high losses and limited integration [6]. Localized Surface Plasmon Resonance (LSPR) concentrates the field but is limited by ohmic losses and fabrication complexity [7]. Laser-Induced Surface Plasmon Polaritons (LASP) offer high speeds but are sensitive to structural defects and thermal management [8]. Photonic Crystals provide advantages through light propagation control and high quality factors, yet are limited by tunability and fabrication precision [9]. Kerr materials, through nonlinear effects, enable multi-level memory and reconfigurability but require high light intensity and are sensitive to noise [10]. Meanwhile, Phase Change Materials (PCMs) enable non-volatile storage and high optical contrast, allowing data retention even after the light source is removed, although they face challenges such as low crystallization speeds and cyclic degradation [11]. Slow-Light techniques enhance light-matter interaction but suffer from

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limited bandwidth and coupling losses [12]. Finally, Semiconductor Optical Amplifiers (SOAs) provide high gain but are limited by polarization sensitivity and gain saturation [13].

Plasmonics, due to its unique ability to confine and control electromagnetic fields at sub-wavelength scales, has become a key platform for the development of integrated optical components [14]. In this regard, the Metal-Insulator-Metal (MIM) waveguide structure is considered one of the prominent architectures, offering high compactness, precise tunability, and compatibility with integrated photonic circuits [15]. It finds applications in the design of various components, including couplers [16], filters [17], logic gates [18], sensors [19], switches [20], and photodetectors [21].

One of the prominent approaches in the development of the next generation of photonic and plasmonic devices is the integration of phase-change materials with advanced platforms such as Silicon-on-Insulator (SOI) [22], CMOS photonics [23], plasmonic structures [24], photonic crystals [25], metasurfaces and metamaterials [26], III-V semiconductor platforms [27], high-refractive-index dielectric nanostructures [28], nano-antenna arrays [29], hybrid 2D graphene structures [30], digital lenses and programmable photonics [31], terahertz band devices [32], and photonic neuromorphic architectures [33].

In the design of plasmonic memories, optical pulses serve as the primary input signals, each characterized by distinct physical parameters. The programming signal consists of RESET and SET pulses; applying these signals to the phase-change material modifies its microscopic structure, inducing a transition between the amorphous and crystalline phases [34].

When the GST material is in the amorphous state, a SET pulse characterized as a low-power (low-amplitude) laser pulse with a relatively long duration is applied. This process reduces the electrical resistance and increases the refractive index as the material transforms into the crystalline state. Conversely, when the material is crystalline, a RESET pulse a high-power (high-amplitude) laser pulse with a relatively short duration is applied. This causes the material to revert to the amorphous state, resulting in increased resistance and a decreased refractive index [35,36].

The energy required for the crystallization of the GST material, initiated by the SET pulse, is estimated at approximately 7.5 pJ. This energy is delivered via a 150 mW pulse over a duration of 150 ns. Conversely, the amorphization process, triggered by the RESET pulse, requires approximately 2.2 pJ of energy, which is supplied by a 110 mW pulse for a duration of 20 ns [37].

In recent years, plasmonic memories incorporating phase-change materials have emerged as a pioneering class of nonlinear optical devices, effectively merging non-volatile storage capabilities with tunable optical responses [38]. By exploiting localized surface resonances and nanoscale phase-change dynamics, these structures provide a robust platform for the implementation of plasmonic neuromorphic synapses [39]. Within these architectures, synaptic weights can be precisely modulated through optical excitation and material phase transitions, which facilitates adaptive learning, analog weight tuning, and parallelized information processing [40]. Such advancements represent a critical milestone toward realizing all-optical neuromorphic computing and the seamless integration of logic and memory functions within a unified photonic platform [41].

Recent developments in non-volatile photonic and plasmonic memories have introduced innovative material systems and coupling mechanisms to achieve low energy consumption and high readout contrast. For instance, a GSST-based phase-change plasmonic memory leveraging dipolar transverse plasmon chain modes along a single-mode waveguide achieved a high optical readout contrast (~80 %) at $\lambda = 1.04$ μm, offering low write and erase energies of 11.5 pJ and 41.4 pJ with rapid switching dynamics (2 ns and 15 ns) [42]. Beyond inorganic phase-change materials, molecular-scale plasmonic memory concepts have also been realized experimentally; an all-plasmonic memory integrating silver nanowires (AgNW) with photochromic diarylethene (DAE) molecules demonstrated sub-diffraction-limit state storage, utilizing reversible refractive index shifts for writing/erasing and non-destructive plasmonic Second-Harmonic Generation (SHG) for state retrieval [43].

Phase-change plasmonic memories have been explored through various design topologies. A non-volatile plasmonic memory based on GST dimer nanoantennas was proposed in [44] and subsequently fabricated using electron-beam lithography, where achieving the target nanoscale gap between nanoantennas was identified as a critical fabrication challenge. However, normalizing the insertion loss (IL) reduced the average transmission error from 25 % to 4.5 % [45]. In a GST ring-based plasmonic memory operating at a resonant wavelength of 1550 nm, an optical transmission contrast of 15.8 % was reported between the crystalline and amorphous states (representing logic '1′ and logic '0′) [46]. Furthermore, phase-change memory designs utilizing plasmonic chain modes demonstrated that high and stable device contrast is maintained even under incomplete state switching [42]. Comprehensive reviews categorize reported parameters across various works, citing extinction ratios in the range of 0.7–16 dB, footprints spanning 1–310 μm^2, and storage densities up to 6 bits/μm^2 [47]. Additionally, on-chip programmability with femtosecond-scale temporal responses has been integrated into racetrack plasmonic resonators based on GST [48], and photonic crystal waveguide crossbars (3 × 3 intersections) have been extended for all-optical neuromorphic synapses [49].

Plasmonic memories based on GST phase-change material fall into the categories of Phase-change Random Access Memory (PRAM) and Non-Volatile Random Access Memory (NVRAM) [50].

Optical neuromorphic computing is an emerging brain-inspired paradigm in which information processing is performed using photons instead of electrons. Optical neural networks, benefiting from high bandwidth, low latency, and low energy consumption, are considered promising candidates for next-generation computing systems. However, one of the main challenges in this field is the implementation of tunable and stable synaptic elements [28,33].

To address these challenges, this paper proposes a non-volatile double-ring MIM plasmonic memory based on a GST phase-change material and silver waveguides, offering an ultra-compact footprint (0.219 μm^2) and an exceptional storage density of 4.56 bits/μm^2 with multi-bit scalability up to 8 bits (256 states). Operating at the resonance wavelength of 1814 nm, the optimized structure delivers a high optical contrast of 87 %, a remarkable extinction ratio of ER = 44.04 dB, and an ultra-low insertion loss of 0.60 dB for logic state '1′ (45.60 dB for logic '0′). The proposed architecture features all-optical external programmability, non-destructive readout, and ultrafast readout dynamics in the femtosecond regime (τ_r = 62 fs). By directly mapping GST material states to quantized transmittance levels, the cell functions as a versatile photonic weighting element for optical neural networks to alleviate the von Neumann bottleneck. Furthermore, we outline a 5-stage BEOL CMOS-compatible fabrication flow (≤200 °C) and demonstrate high fabrication tolerance, where dimensional variations within a ± 5 nm window induce minimal performance fluctuations (ΔER < 1 dB).

The remainder of this paper is organized as follows: Section 2 details the design methodology and theoretical background. Section 3 presents the structural design and numerical performance analysis of the phase-change-based plasmonic memory. Section 4 explores the architectural bit-scaling and expansion of the proposed memory to enhance storage density and data capacity. Section 5 investigates the temporal response analysis and ultrafast optical readout dynamics. Section 6 discusses potential applications in photonic neuromorphic computing and photonic weight arrays. Section 7 outlines nanofabrication considerations, BEOL CMOS integration steps, and structural tolerance analysis. Finally, concludes the study and summarizes the key findings of the proposed memory architecture.

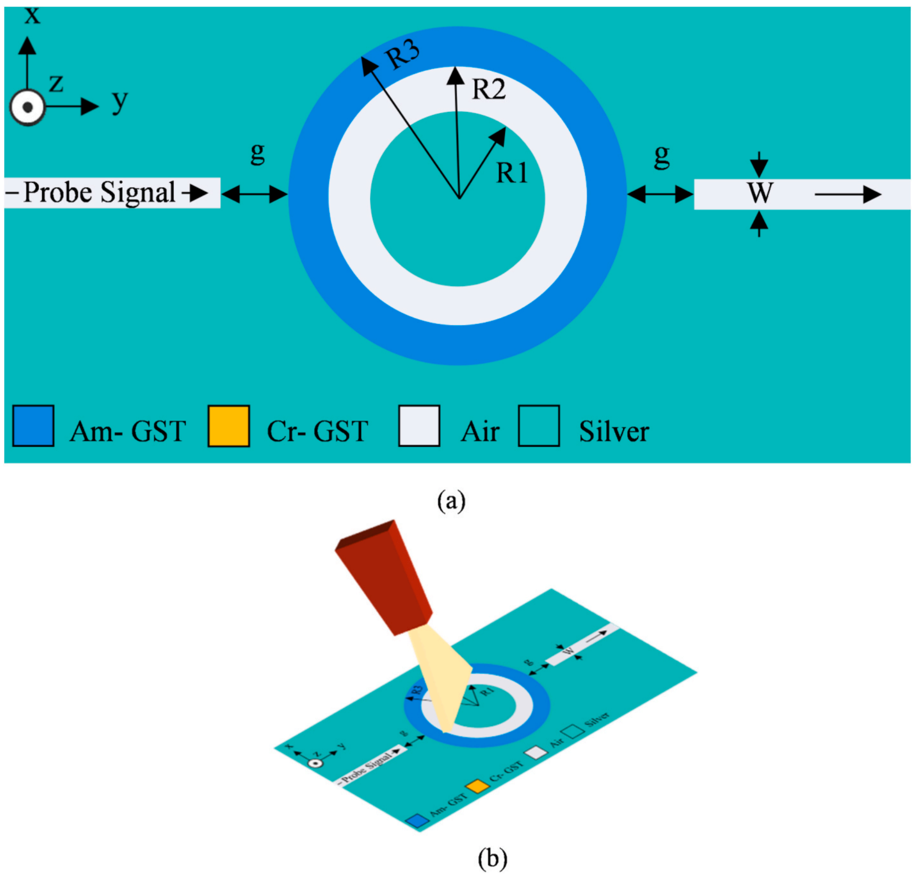

Fig. 1. (a) Schematic configuration of the proposed single-bit disk-shaped plasmonic memory (b) Memory programming based on phase-change GST material using laser excitation to induce reversible transitions between the amorphous and crystalline phases.

Design methodology

SPPs emerge at metal-dielectric interfaces through the coupling of electromagnetic waves with a metal's free electrons. The dispersion relation for the fundamental surface plasmon TM mode can be obtained as follows [51]:

$$K_{spp} = \sqrt{\frac{\varepsilon_d \varepsilon_m(\omega)}{\varepsilon_d + \varepsilon_m(\omega)}}\ \frac{\omega}{c} \tag{1}$$

In Equation (1), k_{SPP} is the plasmonic wave vector, $\varepsilon_m(\omega)$ is the permittivity of the metal, ε_d is the permittivity of the dielectric and c is the speed of light in vacuum. The optical response of noble metals such as silver and gold in plasmonic nanostructures has been modeled using the Drude formalism Equation (2), which describes the free-electron behavior across visible and infrared spectral regimes. $\varepsilon(\omega)$ is the complex dielectric function, ε_∞ is the high-frequency dielectric constant, ω_p is the plasma frequency, γ is the damping constant and $\omega = \frac{2\pi c}{\lambda}$ is the angular frequency of the incident light [52,53].

$$\varepsilon(\omega) = \varepsilon_\infty - \frac{\omega_p^2}{\omega^2 + i\gamma\omega} \tag{2}$$

To calculate complex and continuous models using numerical methods, the structure must be converted into a discrete and simplified model with nanometric dimensions through meshing [54]. By reducing the mesh size, computational accuracy increases, but simulation time also rises [55]. In this work, the mesh size is set to 2 nm. According to Equation (3), the simulation time (T) is proportional to the mesh dimensions (Δx), allowing for the calculation of the simulation duration.

$$T \propto \frac{1}{\Delta x^4} \tag{3}$$

Defining the Perfectly Matched Layer (PML) absorbing region is critical in numerical simulations. This region is used to model infinite space and prevent light from reflecting back into the structure [56]. In the design of the proposed structure, this region is modeled with 100 layers to ensure the reliability of the results. The strip MIM and Y-splitter waveguides have nanometric dimensions and consist of 50 layers.

Plasmonic memory design

In this paper, a non-volatile plasmonic memory based on input and output MIM waveguides and GST phase-change material is proposed. In this design, silver is utilized as the metal, while air and the phase-change material serve as the dielectrics. The Drude model is employed to characterize the dielectric function of the metal, and results are reported using the two-dimensional Finite Difference Time Domain (FDTD) method. In the simulation, a Gaussian pulse with the capability to excite the TM mode is used as the light source, applied to the structure through the input waveguide.

The proposed single-bit plasmonic memory structure consists of an input MIM waveguide, concentric disk and ring resonators, and an output MIM waveguide. The central disk resonator is filled with silver, surrounded sequentially by rings filled with air and GST material. The schematic of the proposed memory structure is illustrated in Fig. 1.

This memory is designed with off-chip programmability, such that a programming signal containing either a SET or RESET pulse is applied to the structure using an external laser. This signal is applied as an optical pulse to determine the phase of the material; depending on the applied

Table 1
Design parameters and dimensions of the disk shaped plasmonic memory cell.

Parameter	R1	R2	R3	g	W
Dimensions (nm)	140	190	240	0	50

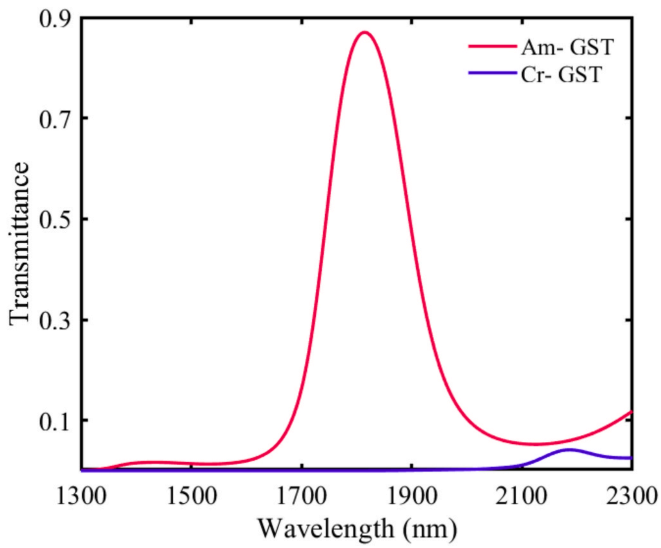

Fig. 2. Transmittance spectra of the memory structure in both amorphous and crystalline phases.

pulse, logic states 0 and 1 are stored in the memory. To read the stored logic state, a low-power (low-amplitude) signal must be utilized. In this design, a probe signal is employed, which is configured such that it cannot induce a change in the refractive index or the material phase. By analyzing the transmittance levels, this signal is capable of distinguishing between logic states 0 and 1. The dimensions of the design parameters are listed in Table 1.

The transmittance curve in the wavelength range of 1300–2300 nm for both amorphous and crystalline states is shown in Fig. 2. By applying the programming signal containing the SET pulse, the GST material transitions to the crystalline state, and the structure exhibits no transmission (zero transmittance). By applying the programming signal containing the RESET pulse, the GST material transitions to the amorphous state. At the resonance wavelength of 1814 nm, the transmittance curve shows a transmittance coefficient of 87 %, a bandwidth (FWHM) of 168 nm, and a quality factor of 10. To achieve these results, optimization of the variable design parameters has been performed.

The proposed structure exhibits the capability to function as a phase-change material-based plasmonic filter. When the GST material is in the amorphous state, the structure acts as a single-mode band-pass plasmonic filter. Conversely, when the GST material is in the crystalline state, the structure functions as a band-stop filter.

$$\text{Contrast} = T_{am}\text{-}T_{cr} \tag{4}$$

$$\text{Extinction Ratio (dB)} = 10\log_{10}\frac{T_{am}}{T_{cr}} \tag{5}$$

$$\text{Storage Density}\left(\frac{\text{bits}}{\text{Î¼m}^2}\right) = \frac{\text{Total Number of Bits}}{\text{Total Area }(\text{Î¼m}^2)} \tag{6}$$

Geometric parameter optimization plays a pivotal role in tailoring the spectral performance and resonance characteristics of plasmonic memory architectures. To establish the optimized structural dimensions for the proposed dumbbell-shaped memory cell, a Parametric Sweep Simulation (PSS) framework was conducted with a fine mesh grid resolution of $\Delta x = \Delta y = 2$ nm. Fig. 3 illustrates the three-dimensional (3D) transmission spectra of the dumbbell-shaped memory cell as a function of variation in two key geometrical parameters, namely the radii R1 and R3.

Across the wavelength spectrum of 1500–2700 nm, the inner radius R1 was swept from 120 nm to 160 nm in increments of 2 nm. As depicted in Fig. 3(a), increasing R1 induces a distinct red-shift (spectral movement toward longer wavelengths) in the resonance dip, attributed to the enlargement of the effective cavity optical path length. Concurrently, the transmission coefficient exhibits an oscillatory trend, initially rising with R1, followed by a gradual decay before increasing again.

Furthermore, the parameter R3 was systematically varied from 220 nm to 260 nm with a step size of 2 nm within the spectral regime of 1000–2500 nm (Fig. 3(b)). The results indicate that increasing R3 yields a non-monotonic modulation of the optical transmittance, where the transmission magnitude rises to a peak value before deteriorating at larger dimensions. Simultaneously, a continuous red-shift in the resonant wavelength is maintained throughout the R3 variation process, confirming the high geometric sensitivity and spectral tunability of the proposed dumbbell plasmonic cavity.

Fig. 4 illustrates the contrast ratio and the extinction ratio (ER) of the memory structure for both amorphous and crystalline states, respectively. These parameters indicate the structure's capability to distinguish between the amorphous and crystalline phases of the GST material and to differentiate between logic states 0 and 1. It is observed that at the resonance wavelength of 1814 nm, the structure achieves a contrast of 87 % and an ER = 44.04 dB. These results are calculable using Equations

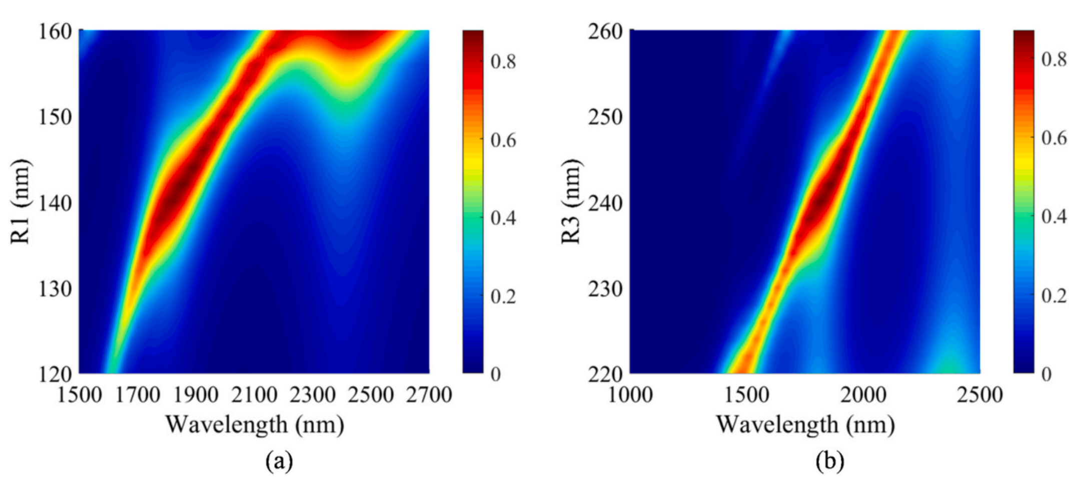

Fig. 3. Three-dimensional transmission curves of the double-ring memory versus dimensional variations: (a) R1, and (b) R3.

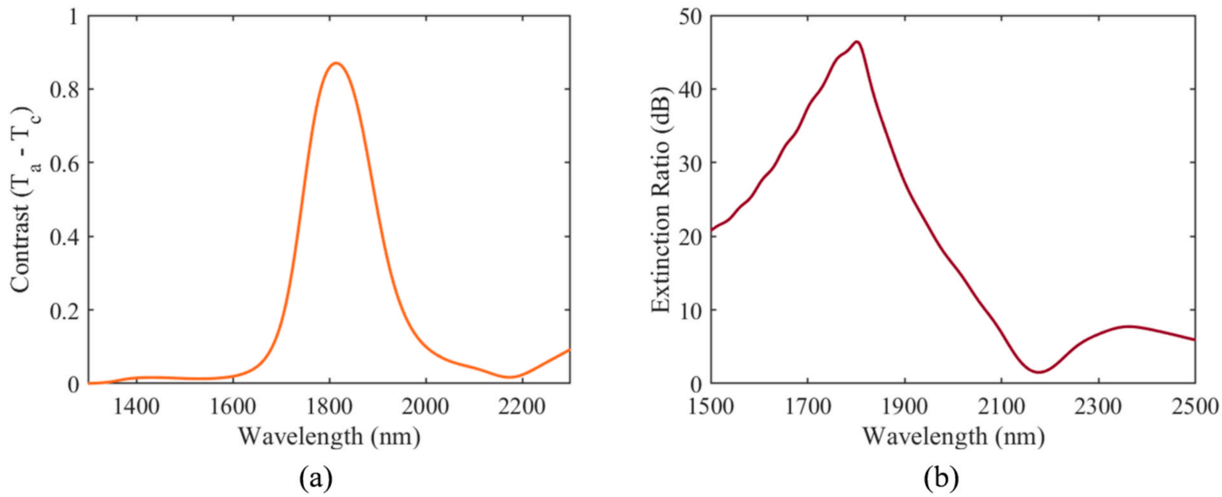

Fig. 4. (a) Contrast ratio and (b) Extinction Ratio (ER) as a function of wavelength.

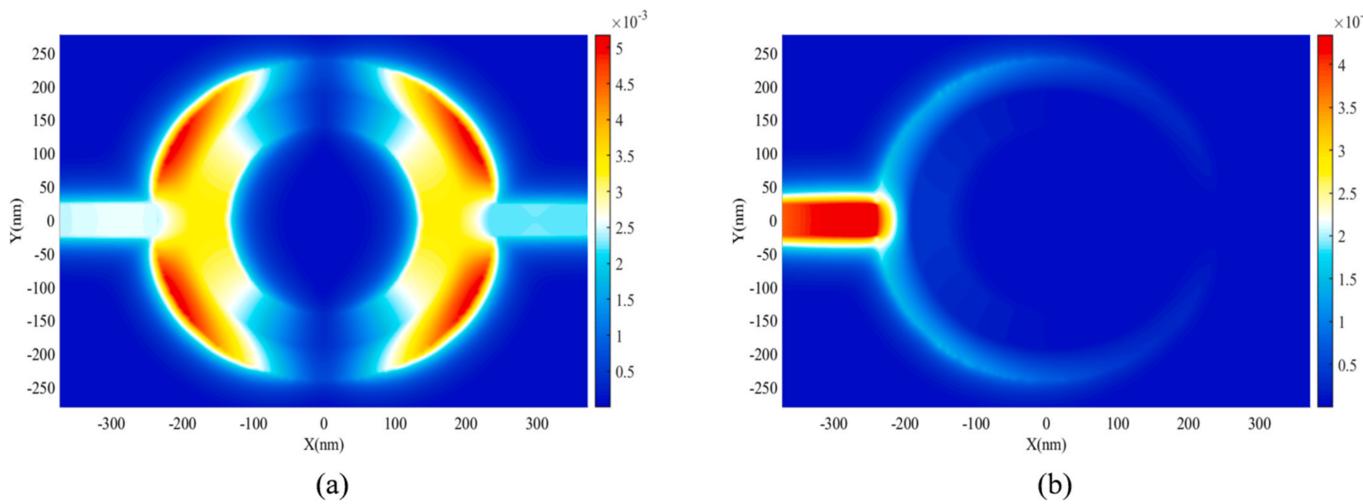

Fig. 5. Magnetic field distribution magnitude of Re |H| during the read operation for (a) Logic state 1 and (b) Logic state 0.

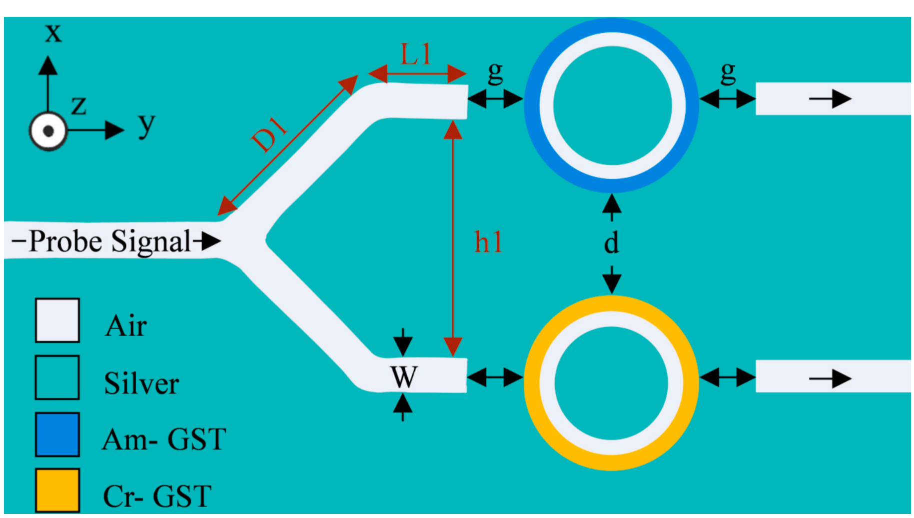

Fig. 6. Schematic of the 2-bit memory architecture based on an MIM Y-splitter waveguide.

(4) and (5).

The magnetic field magnitude (H) distribution at the resonance wavelength for both amorphous and crystalline states is shown in Fig. 5. It is observed that in the amorphous state, due to low absorption losses,

Table 2
Geometric dimensions of the variable parameters (L, D, and h) for the Y-splitter MIM waveguides in 2-bit, 4-bit, and 8-bit configurations.

Parameter	L1	D1	h1	L2	D2	h2	L3	D3	h3
Dimensions (nm)	50	320	460	50	320	970	50	320	1990

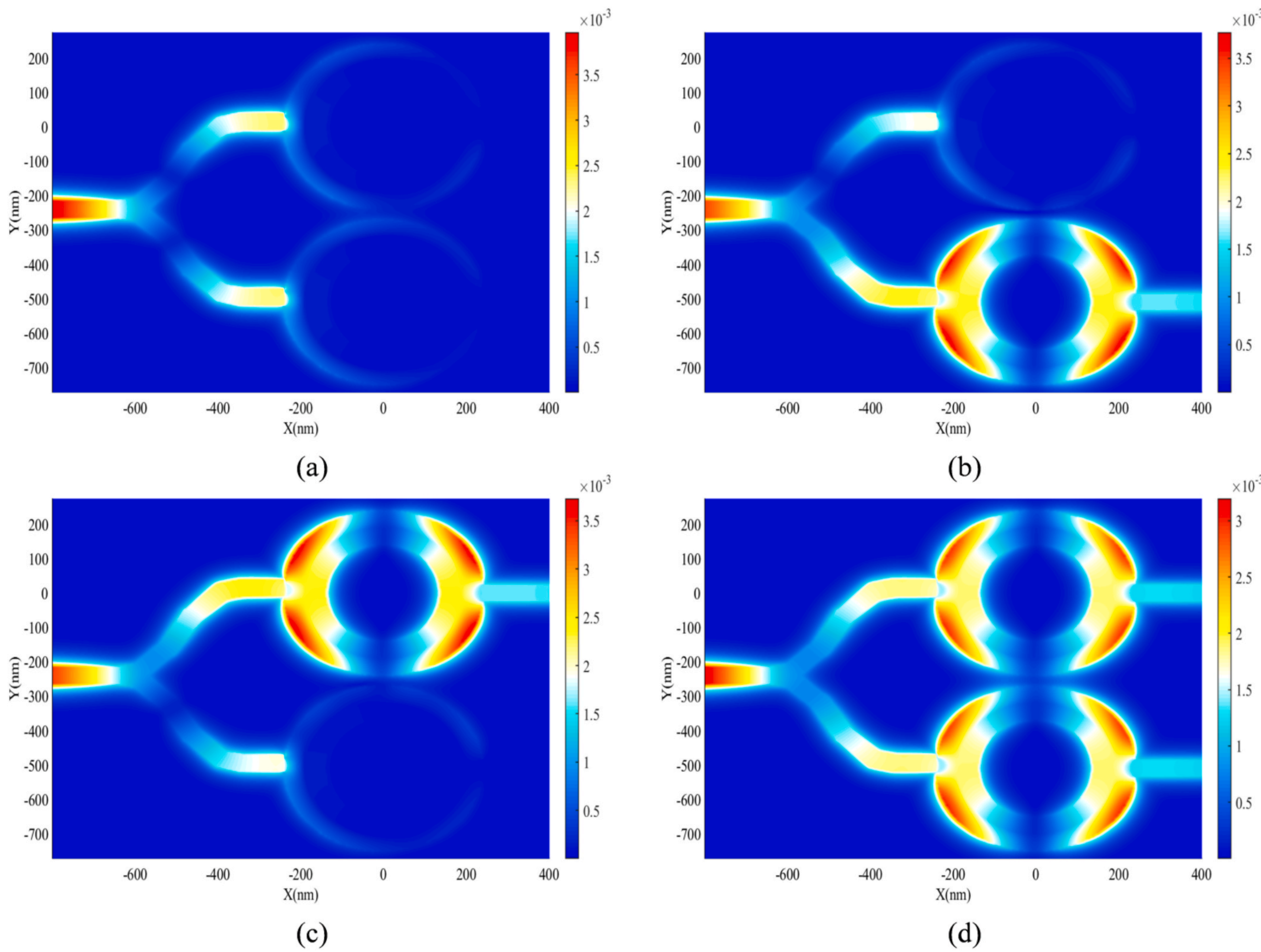

Fig. 7. Magnetic field magnitude of Re |H| profiles for reading logic states: (a) 00, (b) 01, (c) 10, and (d) 11.

the magnetic field is capable of circulating within the resonator. This circulation induces the resonance phenomenon, resulting in maximum signal transmission to the output [50], which justifies the read operation of logic state 1. In the crystalline state, due to high absorption losses, the magnetic field is rapidly attenuated, and no signal is transmitted to the output [57], which justifying the read operation of logic state 0. This single-bit memory has a footprint of 0.219 Î¼m^2 and a density of 4.56 $\frac{\text{bits}}{\text{Î¼m}^2}$, which is calculable using Equation (6).

The neuromorphic functionality of the proposed plasmonic memory can be directly inferred from its phase-dependent optical response. A pronounced difference in optical transmission at the resonance wavelength of 1814 nm between the amorphous and crystalline phases of the GST material provides an effective mechanism for precise modulation of the output intensity. This feature enables a direct mapping of optical intensity to synaptic weights in neuromorphic systems, supported by a high contrast of approximately 87 % and an extinction ratio of 44.04 dB, ensuring reliable distinguishability between different states.

Within this framework, the amorphous phase, characterized by higher transmission, corresponds to a potentiated synaptic state, whereas the crystalline phase, with lower transmission, represents a depressed synaptic state. Moreover, time-domain analysis reveals that the transient response is not limited to binary switching but allows for continuous and gradual tuning of synaptic weights. This behavior arises from the strong coupling between plasmonic resonances and the phase-change dynamics of the material, highlighting the capability of the proposed structure to function as an all-optical synaptic element for neuromorphic computing applications.

To accurately evaluate the integration potential of the proposed memory architecture, we distinguish between the active cell footprint and the effective total unit-cell area required in a photonic integrated circuit (PIC). The storage density is calculated based on the relation given in Equation (6).

The active memory cell—comprising the GST-filled plasmonic rectangular resonator—occupies an extremely compact footprint of 0.219 μm^2, corresponding to an active storage density of 4.56 bits/μm^2 evaluated via Equation (6).

For practical high-density integration, the overall spatial footprint of

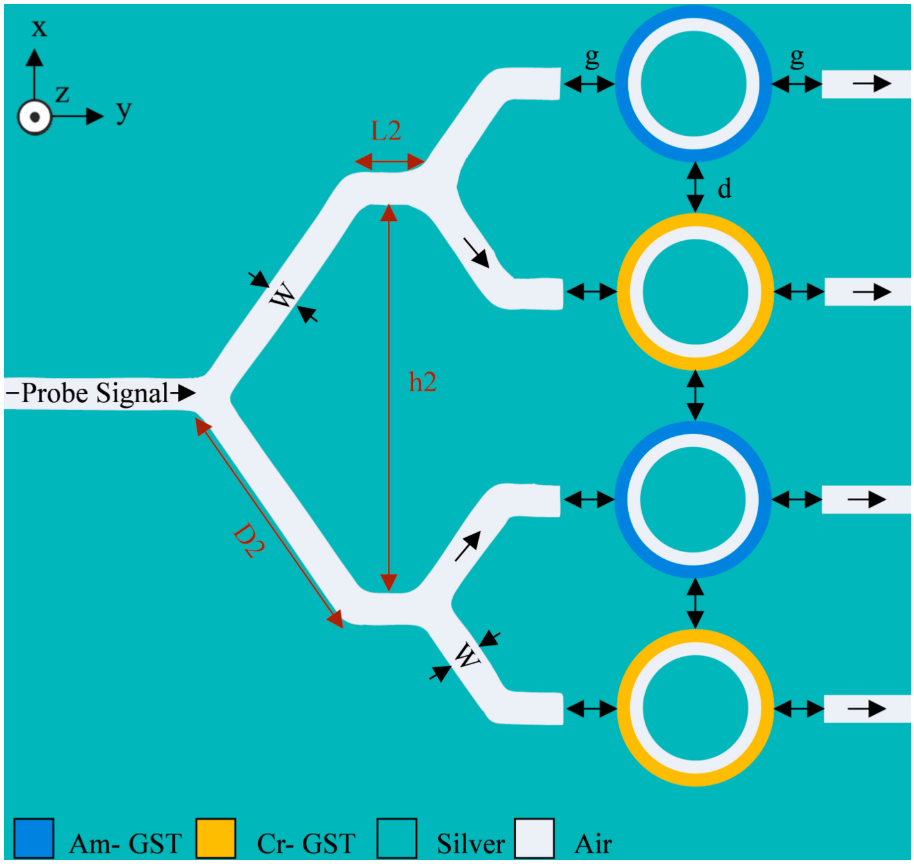

Fig. 8. Schematic of the 4-bit plasmonic memory based on a tree-structured power divider arrangement.

a functional unit cell must also incorporate the essential MIM coupling waveguides and the spatial isolation boundaries required to suppress crosstalk between adjacent bits. Accounting for these complete functional boundaries (0.219 μm^2), the effective total footprint yields a realistic circuit-level storage density of 4.56 bits/μm^2 according to Equation (6).

Owing to the external top-illumination scheme used for optical programming, the design avoids the spatial overhead of integrated electrical contact lines or individual micro-heaters. Combined with the strong optical field confinement provided by the etched air-groove MIM topology in the silver film, this ultracompact footprint demonstrates the high feasibility of the proposed design for ultra-dense all-optical memory arrays.

Design generalization for memory density enhancement

In plasmonic memories, achieving multi-bit memory arrays is of paramount importance. In this paper, two, four, and eight-bit memories based on the plasmonic memory cell introduced in Section 3 are sequentially designed and proposed.

Fig. 6 illustrates the schematic of the two-bit memory structure in the logic state "10″. An MIM waveguide with a Y-splitter schematic is utilized to distribute the probe signal between the two memory cells. An ideal Y-splitter is capable of dividing the input power equally (50 %) between the two output waveguides; however, in practice, due to losses, less than 50 % of the input probe signal is transmitted to each output waveguide [58]. Generally, the use of power dividers offers several advantages, including reduced footprint, isolation between signals, uniformity of power distribution, and increased speed and synchronization of operations across multiple memory cells [59]. Given that the probe signal is a low-power (low-amplitude) signal that cannot alter the refractive index or the material phase, distributing this signal through power splitters causes a significant drop in its power (amplitude), which may hinder its efficiency in detecting and distinguishing between the amorphous and crystalline states. Increasing the input power is proposed as a feasible implementation option [58]. In the two bit memory design, the probe signal power for each memory cell must remain unchanged relative to the single-bit design. Therefore, to achieve this, the input probe signal power must be doubled. Table 2 lists the dimensions of the variable parameters for the MIM waveguides with Y-splitter schematics for the two-, four-, and eight-bit memories, respectively.

The magnetic field magnitude (H) distribution corresponding to logic states 00, 01, 10, and 11 is shown in Fig. 7, respectively. It is observed that in the amorphous state, due to low absorption losses, the cells appear "on" (bright), justifying the read operation of logic state 1. In the crystalline state, due to high absorption losses, the cells appear "off" (dark), representing the read operation of logic state 0.

By combining two 2-bit memory units and a Y-splitter waveguide, the 4-bit plasmonic memory structure in logic state 1010 is illustrated in Fig. 8. Utilizing power dividers in a tree-like configuration yields lower losses compared to a series configuration [58]. In this design, one power divider is used in the first stage and two power dividers are used in the second stage to distribute the input probe signal. To deliver a probe signal with the same power level as that applied to the single-bit memory structure, the input probe signal power must be increased by a factor of four.

The magnetic field magnitude (H) distribution of the 4-bit plasmonic memory for various logic states is shown in Fig. 9. Memory cells in logic state 1 are depicted as "on" (bright), while cells in logic state 0 are shown as "off" (dark).

By combining two 4-bit memory units and a Y-splitter waveguide, an 8-bit plasmonic memory structure can be achieved. To minimize power losses, a tree-like arrangement of power dividers is utilized, and the input probe signal power is increased by a factor of eight. The

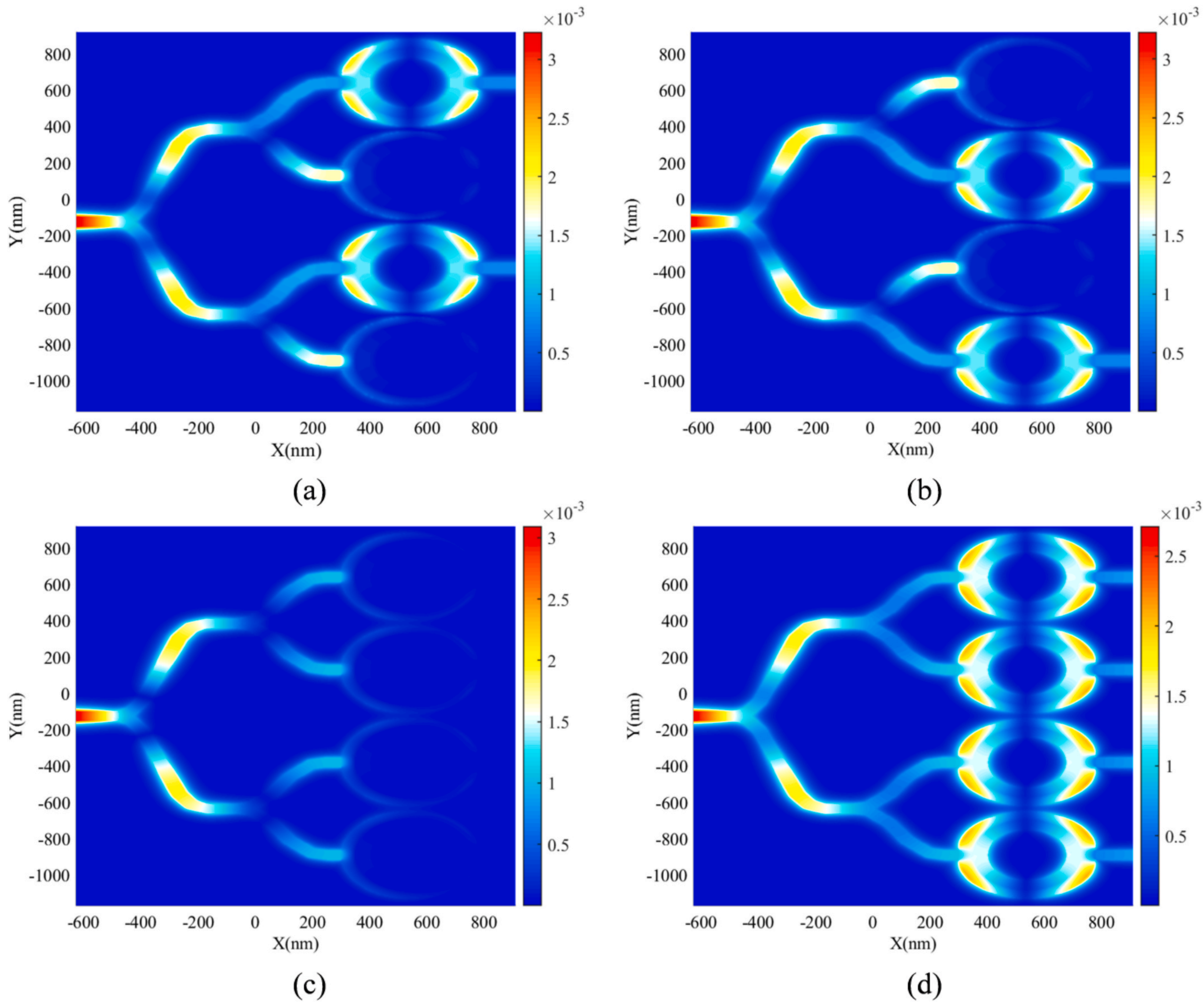

Fig. 9. Magnetic field magnitude of Re |H| distributions for 4-bit memory read operations: (a) 1010, (b) 0101, (c) 0000, and (d) 1111.

dimensions of this waveguide are listed in Table 2 under the parameters L3, D3, and h3, respectively. Fig. 10 displays the magnetic field magnitude (H) distributions for the 8-bit memory at the resonance wavelength of 1814 nm for two different logic states.

In this work, the scalability of the proposed memory structure has been systematically investigated by extending it from a single-bit configuration to multi-bit architectures, including 2-bit, 4-bit, and ultimately 8-bit implementations. This progressive scaling demonstrates that the proposed design possesses strong expandability and is capable of supporting multiple stable states. As the number of bits increases, the number of accessible states grows exponentially.

The increase in memory cells up to the 8-bit level is not merely a matter of enhanced storage capacity; rather, it plays a crucial role in improving neuromorphic performance. In neuromorphic architectures, the precision of synaptic weight representation is of fundamental importance. A higher number of distinguishable levels enables more accurate modeling of biological synaptic behavior. In this context, transitioning from limited discrete states to an 8-bit multilevel space significantly enhances weight resolution, thereby improving both learning accuracy and the generalization capability of the network.

Furthermore, the presence of diverse logical states within a multibit framework enables the simultaneous implementation of logical operations and synaptic computations, reducing the need for separate processing modules. Combined with the ability for gradual weight tuning, this leads to improved efficiency in implementing learning algorithms, particularly in deep learning and parallel processing applications. Additionally, increasing the number of bits contributes to an improved signal-to-noise ratio and reduced quantization error, ultimately enhancing the stability and accuracy of the neuromorphic system.

To quantify optical signal degradation during readout operations, the Insertion Loss (IL) of the proposed double-ring plasmonic memory is evaluated at the resonant wavelength of $\lambda = 1814$ nm based on Equation (7):

$$\text{Insertion Loss (dB)} = -10\log_{10}T \tag{7}$$

Fig. 11 presents the calculated insertion losses for both logic '1′ (amorphous state) and logic '0′ (crystalline state) readout across 1-, 2-, 4-, and 8-bit memory architectures. For the baseline 1-bit memory cell, the structure exhibits an insertion loss of 0.60 dB in the logic '1′ state and an attenuation of 45.60 dB in the logic '0′ state.

As the memory architecture scales to higher bit resolutions, the logic '1′ insertion loss increases due to cumulative plasmonic propagation

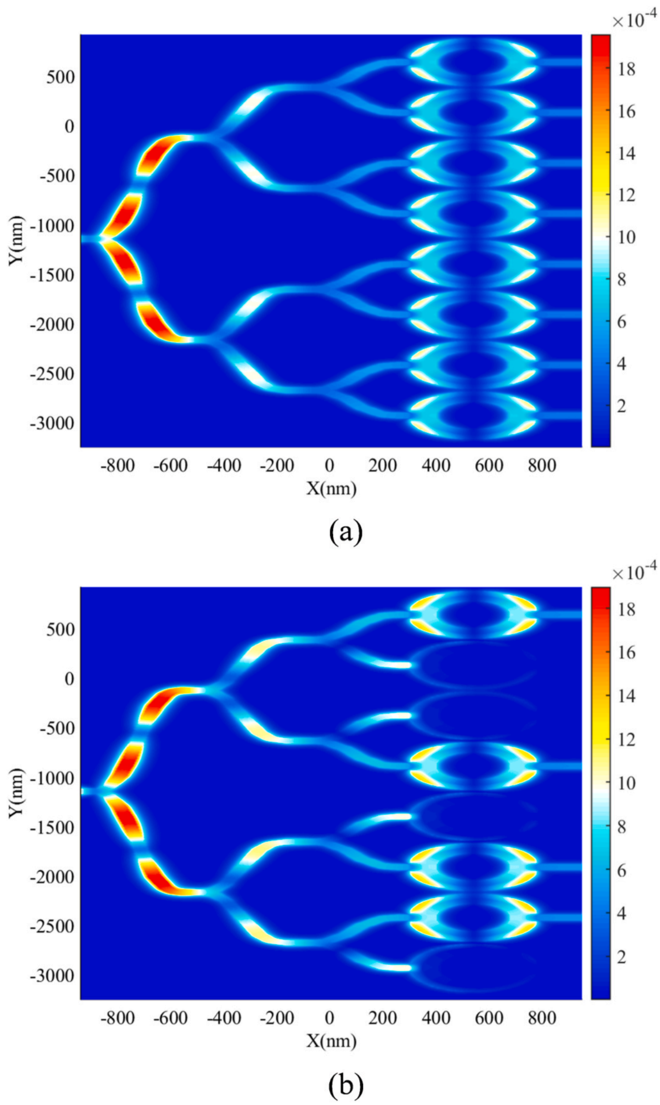

Fig. 10. Magnetic field magnitude of Re |H| profiles of the 8-bit memory at $\lambda = 1814$ nm for states: (a) 11,111,111 and (b) 10010110.

losses and cavity coupling overhead, yielding 5.44 dB for the 2-bit, 9.12 dB for the 4-bit, and 14.09 dB for the 8-bit configuration. Conversely, the logic '0′ state maintains high signal attenuation, recording levels of 45.38 dB, 52.21 dB, and 57.62 dB for the 2-, 4-, and 8-bit designs, respectively. Overall, the memory structure demonstrates a high optical contrast of 87 % and an extinction ratio of ER = 44.04 dB, ensuring clear state discrimination during non-destructive optical readout.

Temporal response analysis and ultrafast optical readout dynamics

To evaluate the dynamic readout response, transient coupling, and power stabilization of the proposed memory structure under real operating conditions, a time-domain analysis was conducted using a normalized square probe pulse, as illustrated in Fig. 12(a). It should be emphasized that this time-domain simulation characterizes the optical readout dynamics (i.e., optical propagation and cavity field setup time for a fixed material state) and is fundamentally distinct from the thermal phase-change switching kinetics (write/erase operations) of GST, which typically occur on the nanosecond (ns) timescale.

Upon applying the probe pulse to the input waveguide, the temporal response of the double-ring memory for both binary states is shown in Fig. 12(b) and 12(c). In the amorphous GST state ('1′ state), the temporal response closely tracks the input probe signal with a minimal propagation delay of 7 fs. During the 107–200 fs interval, transient behavior at the rising edge is observed, corresponding to the optical energy coupling time required to establish plasmonic resonance within the double-ring microcavity. Subsequently, the transmitted power stabilizes at a steady-state value of 0.98 within the 200–800 fs window, followed by an exponential decay from 800–900 fs. Based on the 0.98 steady-state level, the measured 10 %–90 % rise time is 62 fs (occurring between 112 fs and 174 fs), and the 90 %–10 % fall time is 53 fs (between 815 fs and 868 fs).

For the crystalline GST state ('0′ state), the probe beam encounters high absorption losses, resulting in a drastically reduced steady-state transmission of 0.007. In this state, the 10 %–90 % rise time and 90 %–10 % fall time are calculated as 24 fs (117–141 fs) and 50 fs (831–881 fs), respectively. The significant transmission contrast between the two phases confirms reliable readout resolution. These femtosecond-scale rise and fall times demonstrate the ultrafast non-destructive readout capability and short photon lifetime of the plasmonic resonator during state interrogation, while the state programming speed remains governed by the nanosecond thermal response of GST.

In Table 3, a comparison is presented between plasmonic memories based on Kerr nonlinear materials and GST phase-change materials. This comparison demonstrates that the proposed memory outperforms previous designs in all key parameters, including Contrast, Insertion Loss, and Extinction Ratio (ER). This superiority highlights the high capability of the current design in detecting and distinguishing between logic states zero and one.

Potential applications in photonic neuromorphic computing

Extensive experimental studies on chalcogenide phase-change materials have demonstrated that, in addition to non-volatile binary switching, GST can access multiple stable intermediate states by precisely controlling fractional crystallization under thermal, electro-thermal, or optical excitation. This multi-level transition capability renders GST a highly promising material platform for multi-bit data storage, optical memristors, and photonic neuromorphic architectures [65–67].

In this paper, a reconfigurable non-volatile plasmonic memory and single-mode bandpass filter based on GST are presented. Evaluating the key performance metrics of the proposed architecture highlights its competitive performance compared to previously reported designs. The non-volatile optical contrast between the amorphous and crystalline GST states allows direct mapping of material states to quantized synaptic weights—where the high-transmission amorphous state represents a strong weighting factor and the suppressed crystalline state represents a weak weighting factor.

Consequently, the presented structure functions not only as a high-density non-volatile optical memory featuring ultrafast femtosecond-scale readout dynamics, but also—by potentially exploiting fractional GST phase transitions in future implementations—as a versatile photonic weighting element (binary or multi-bit) for optical neural networks (ONNs). These findings position the proposed topology as a promising candidate for multifunctional integrated photonic circuits and high-speed optical computing systems.

The operation of the proposed double-ring plasmonic memory relies on the non-volatile phase transition of GST, which retains its structural state without continuous energy input. During state retrieval, a low-power optical probe pulse is launched into the structure. Because the energy density of the readout probe is maintained below the thermal threshold required for phase transformation, the optical readout operation remains entirely non-destructive, ensuring repeatable synaptic weight evaluation in photonic neuromorphic hardware.

The memory exhibits high state differentiation during readout, achieving an optical contrast of 87 % and an extinction ratio of ER =

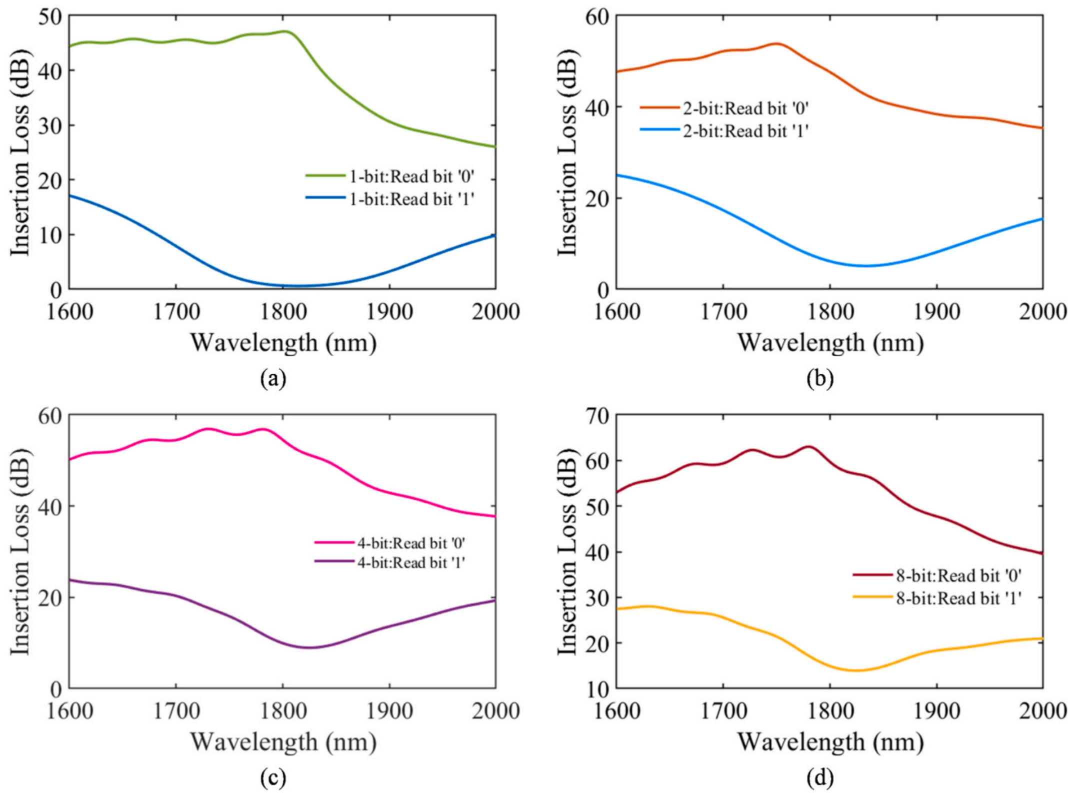

Fig. 11. Calculated Insertion Loss (IL) for logic '1′ and logic '0′ states across 1-bit, 2-bit, 4-bit, and 8-bit memory configurations at $\lambda = 1814$ nm.

44.04 dB, with logic '1′ and '0′ insertion losses of 0.60 dB and 45.60 dB, respectively. These transmission levels provide stable, well-separated optical weight states. Coupled with an ultrafast readout response (62 fs rise time), an ultracompact footprint (0.219 μm^2), and a high effective storage density (4.56 bits/μm^2), the presented architecture offers a promising building block for non-volatile optical memristors and photonic synaptic weighting elements in ultra-high-bandwidth optical neural networks.

To evaluate the scalability and multi-bit data storage capability of the proposed non-volatile GST-based plasmonic memory, the baseline unit-cell architecture was systematically generalized from a 1-bit resolution up to an 8-bit configuration. This multi-bit realization demonstrates distinct, resolvable optical transmission levels, yielding 256 (2^8) stable quantized states that significantly enhance effective storage density and structural integration within photonic integrated circuits (PICs).

These discrete optical transmission states allow the proposed binary and multi-bit memory cells to function as effective photonic weighting elements in optical neural network (ONN) architectures, where static optical transmittance modulates signal power analogously to discrete synaptic weight multiplication. However, it should be clarified that while fractional crystallization in GST can enable continuous multi-level phase control, the primary focus of this work is architectural bit-scaling rather than dynamic fractional phase transition tuning. Consequently, the proposed topology is positioned as a high-density, non-volatile optical weighting array rather than a fully dynamic optical synapse with real-time adaptive learning capabilities.

Nanofabrication considerations and practical tolerances

The architecture of the proposed non-volatile plasmonic memory is tailored for smooth compatibility with conventional Back-End-of-Line (BEOL) CMOS fabrication workflows. Fig. 13 outlines the step-by-step nanofabrication sequence:

- Substrate Preparation and Buffer Isolation: A high-quality 100 nm SiO_2 insulating layer is thermally grown on an RCA-cleaned silicon (Si) wafer via dry oxidation at 1000 °C.
- Metallization Stage: A thin 5 nm titanium (Ti) adhesion film followed by a 100 nm bottom silver (Ag) layer is deposited using electron-beam physical vapor deposition (EB-PVD) under ultra-high vacuum conditions ($<10^{-7}$Torr) at a controlled deposition rate (0.5 Å/s) to achieve sub-nanometer surface smoothness (RMS < 1 nm).
- Nanopatterning and Dry Etching: A central 50 nm Ag film is coated with PMMA resist and patterned using high-precision electron-beam lithography (EBL) with an alignment accuracy below 10 nm. Reactive Ion Etching (RIE) utilizing a CF_4/Ar plasma (50–100 W RF bias) anisotropically defines the double-ring resonator and waveguide layout. The monolithic zero-gap (g = 0 nm) coupling design removes inter-component overlay margins, simplifying patterning to a single lithographic cycle.
- Active PCM Deposition: Radio-frequency (RF) magnetron sputtering is employed to selectively deposit GST into the core cavity, followed by a lift-off step combined with gentle Ar ion beam milling.
- Encapsulation and Upper Metallization: A 100 nm top Ag layer is deposited to finalize the MIM stack, after which a 20 nm conformal Al_2O_3 passivation coat is applied via Atomic Layer Deposition (ALD) at 100 °C to mitigate silver oxidation.

Notably, the thermal budget across all post-substrate operations remains strictly below 200 °C, well underneath the standard 400 °C threshold allowed for BEOL CMOS processing. Furthermore, photothermal phase conversion (SET ≈ 450°K, RESET ≈ 850-900°K) takes place locally via nanosecond optical pulses within deep-subwavelength domains, where the encompassing Ag region functions as an efficient heat dissipater to suppress thermal interference between adjacent components.

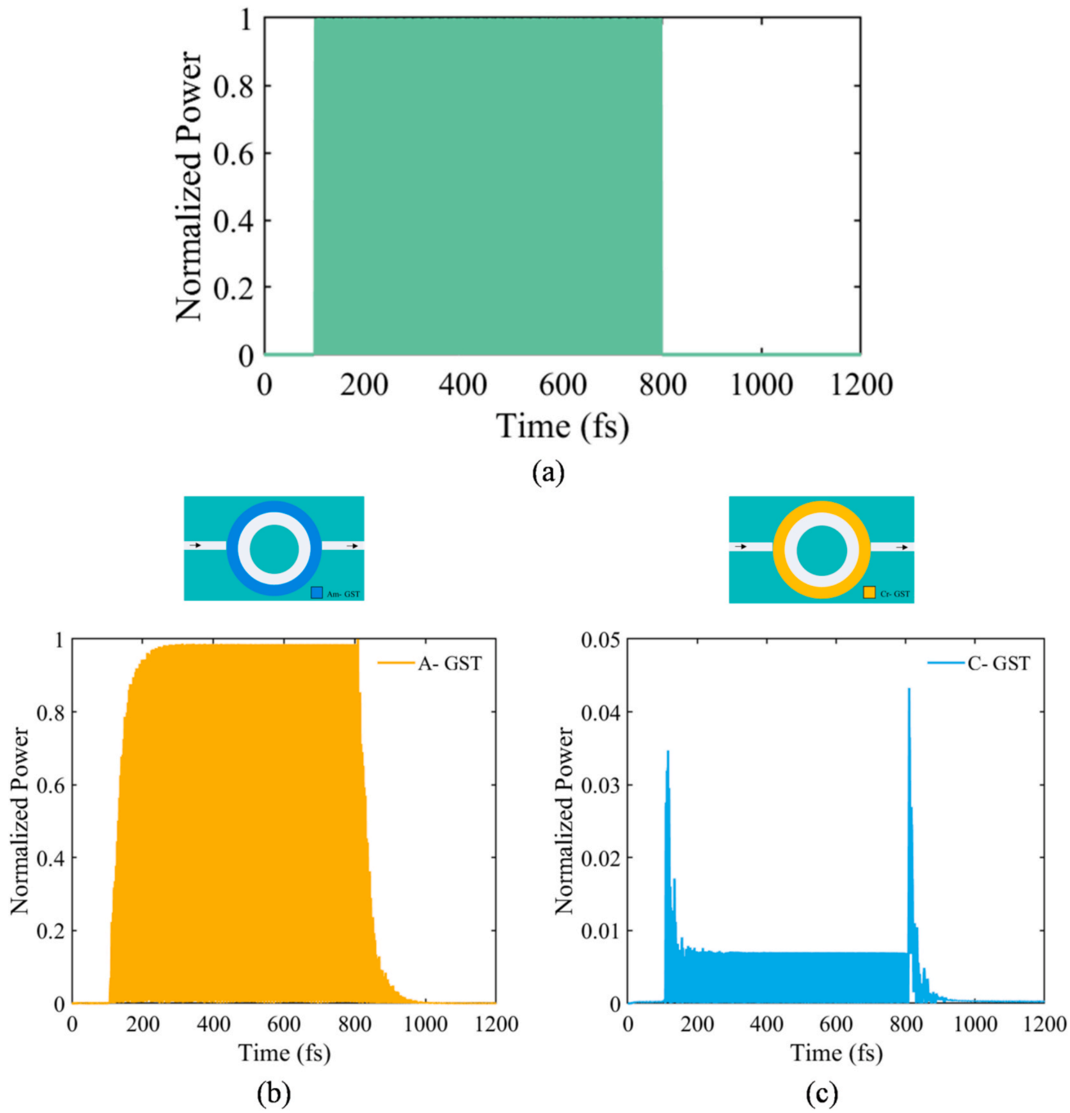

Fig. 12. Time-domain performance of the memory unit cell during optical readout: (a) Normalized input probe signal, (b) temporal response for the amorphous state ('1′ logic), and (c) temporal response for the crystalline state ('0′ logic).

Table 3
Performance comparison between the proposed plasmonic memory and previously reported research (Kerr-based and PCM-based).

Year	Ref	Material	Simulation	λ (nm)	Contrast(%)	ER (dB)	IL (dB)	Footprint (μm^2)
2020	[60]	Kerr	Plasmonic	708	64	10.06	–	0.83
2020	[61]	Kerr	Plasmonic	755	62	15.05	–	0.23
2021	[20]	Kerr	Plasmonic	1485	49	12.38	2.83	0.31
2022	[46]	GST	Plasmonic	1550	15.8	–	A:2.3C:1	0.0045
2025	[62]	GST	Plasmonic	1598	67	–	–	0.031
2025	[63]	GST	Plasmonic	1178	74	–	–	0.14
2025	[64]	GST	Plasmonic	1550	47	4.1	3.41	–
2026	[48]	GST	Plasmonic	1776	84	43.66	Read: A:7.86C:27.86	0.09
2026	[49]	GST	Photonic Crystal	1550	80	0.28	−49	14.8
Proposed Memory		GST	Plasmonic	1814	87	44.04	1-bit: Read: A:0.60C:45.60 2-bit: Read: A:5.44C:45.38 4-bit: Read: A:9.12C:52.21 8-bit: Read: A:14.09C:57.62	0.219

Numerical modeling assumptions vs. practical non-idealities

To evaluate physical device behavior beyond idealized numerical boundaries, three key modeling assumptions and potential experimental variations must be highlighted:

- Dimensionality Considerations (2D vs. 3D Modeling): The proposed memory cell was evaluated using two-dimensional Finite-Difference Time-Domain (2D-FDTD) simulations, providing a computationally efficient framework for analyzing in-plane electromagnetic field behavior. However, 2D models cannot fully capture out-of-plane

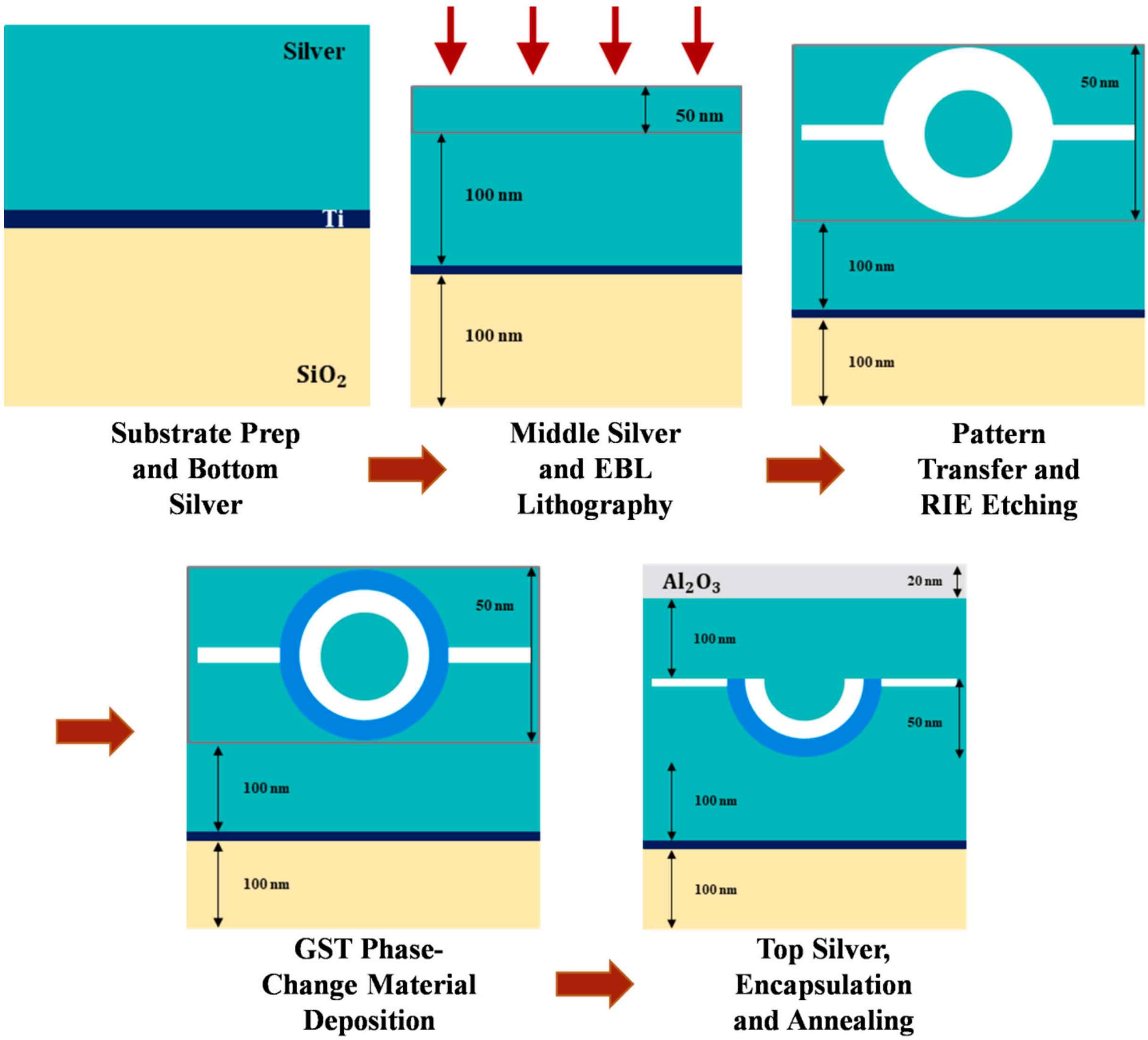

Fig. 13. Schematic and cross-sectional views of the five primary nanofabrication stages of the double-ring plasmonic memory architecture, highlighting substrate preparation, sequential silver depositions, EBL nanopatterning, selective GST deposition, and final protective encapsulation.

scattering losses, vertical mode confinement, and three-dimensional spatial mode distributions. Consequently, minor quantitative discrepancies in absolute transmission values and resonance quality factors may occur when comparing 2D results to full 3D models. Nevertheless, the underlying physical mechanisms, resonance conditions, and phase-dependent optical switching remain intact, as they are fundamentally driven by in-plane plasmonic mode interactions.

- Material Losses and Surface Roughness: The dispersion characteristics of silver were modeled using the Drude dispersion relation. While this model accurately describes high-quality free-electron responses, physically fabricated structures experience supplementary attenuation due to grain boundary scattering, surface roughness, structural defects, and localized oxidation. These real-world non-idealities typically introduce additional optical absorption and scattering losses, leading to slight reductions in transmittance levels, Extinction Ratio (ER), and resonance sharpness without fundamentally altering the core operational principles.
- Inhomogeneous GST Phase Transitions: Numerical models assume uniform phase state distribution across the active material. In physical devices, however, local thermal gradients and heat dissipation patterns can induce partial or non-uniform phase switching. Such fractional phase transitions produce intermediate optical constants (situated between the fully amorphous and fully crystalline limits), enabling multi-level optical transmission states rather than strictly binary operation. While this study focuses on baseline performance using full structural phase boundaries, fractional crystallization provides enhanced opportunities for multi-bit data storage and analog synaptic weight modulation in optical computing hardware.

To evaluate the structural robustness and operational stability of the double-ring plasmonic memory against potential lithographic and etching non-idealities, a parametric sensitivity analysis was conducted. Considering a discretization mesh grid of $\Delta x = \Delta y = 2$ nm, a variation range of $\pm$ 4 nm (representing twice the minimum numerical grid resolution) was individually applied to radii R1, R2, and R3 (Fig. 14).For the baseline parameter R1 = 140 nm, applying a $\pm$ 4 nm tolerance window yields perfectly overlapping extinction curves at the operating resonance wavelength ($\lambda = 1814$ nm), maintaining the nominal value of ER = 44.04 dB. This indicates absolute immunity of R1 against fabrication imperfections. For R2 = 190 nm, a -4 nm deviation enhances the extinction ratio to 48.20 dB, while a + 4 nm deviation reduces it to 38.81 dB, identifying R2 as the primary critical parameter requiring

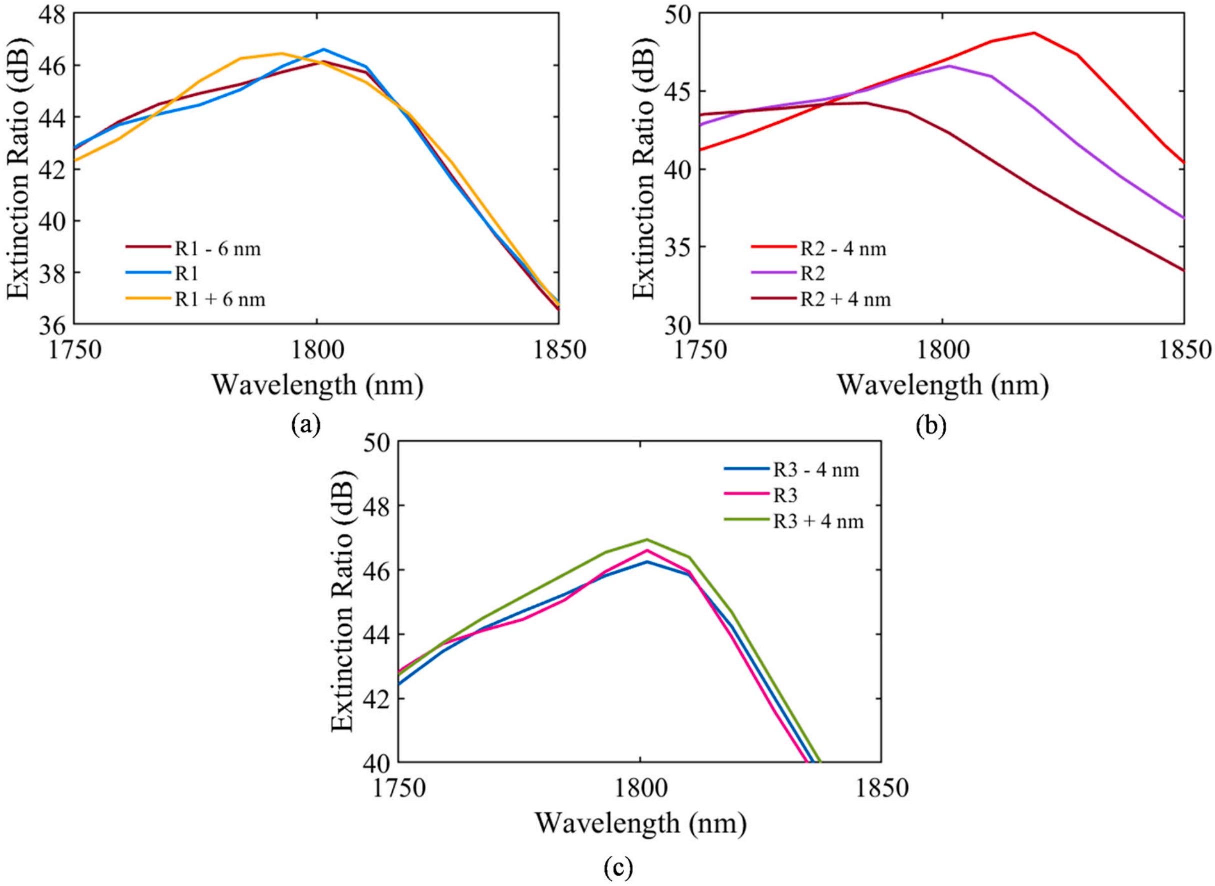

Fig. 14. Extinction Ratio curves and sensitivity analysis under fabrication tolerances for dimensional parameters: (a) R1, (b) R2, and (c) R3 at $\lambda = 1814$ nm.

precise lithographic alignment. Finally, for R3 = 240 nm, dimensional shifts of −4 nm and + 4 nm lead to extinction ratios of 43.91 dB and 44.06 dB, respectively. Because the total fluctuation for R3 remains well below 1 dB, the proposed architecture demonstrates high overall fabrication tolerance under realistic nanomanufacturing conditions.

Conclusion

In this paper, a non-volatile plasmonic memory architecture based on chalcogenide phase-change materials (GST) is proposed and numerically investigated. By generalizing the baseline design, multi-bit memory configurations with 1-, 2-, 4-, and 8–bit resolutions were implemented, demonstrating distinct, resolvable optical transmission states. Specifically, the 8-bit resolution configuration provides 256 (2^8) stable, quantized optical transmission levels with high readout contrast.

These discrete transmission states allow the proposed binary and multi-bit memory cells to serve as effective photonic weighting elements in optical neural networks (ONNs), where the static optical transmittance modulates signal power analogously to applying a discrete synaptic weight factor. While extending this topology to emulate a fully dynamic optical synapse—capable of real-time biological plasticity—remains an important subject for future multi-level phase-control research, the proposed design achieves an optical contrast of 87 % and an extinction ratio of 44.04 dB. Overall, the ultracompact unit-cell footprint, high optical contrast, and ultrafast femtosecond-scale readout latency establish this plasmonic memory design as a promising candidate for high-density optical data storage and integrated photonic weight arrays.

Ethical approval statement

The authors confirm that the submitted paper has not been submitted to any other journal and that this version is original and has not been published elsewhere. Additionally, all listed authors affirm the integrity of the study, data, information, and analyses, ensuring that no manipulations have been made. Furthermore, we confirm that no other individuals meet the authorship criteria for this paper beyond those listed as authors.

CRediT authorship contribution statement

Melina Kehtarmanesh: Writing – original draft, Software, Investigation, Data curation. **Parviz Keshavarzi:** Validation, Supervision, Project administration. **Mohammad Danaie:** Writing – review & editing, Validation, Supervision, Project administration, Conceptualization.

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Declarations

AI tools were used to improve the English content of this paper.

Author agreement statement

We the undersigned declare that this manuscript is original, has not been published before and is not currently being considered for publication elsewhere. We confirm that the manuscript has been read and approved by all named authors and that there are no other persons who satisfied the criteria for authorship but are not listed. We further confirm that the order of authors listed in the manuscript has been approved by all of us. We understand that the Corresponding Author is the sole contact for the Editorial process. He is responsible for communicating with the other authors about progress, submissions of revisions and final approval of proofs.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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